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# Claims

[c1] 1. A method for forming semiconductor structures, the method comprising the steps of:
(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:
(i) forming a first region and a second region, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface, and
(ii) depositing a growth material simultaneously on top of the first and second regions so as to grow third and fourth regions from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface,
wherein the first and third regions comprise a same material and have single-crystal atoms arrangement,
wherein the first region has a different atoms arrangement than the fourth region, and
wherein the step of depositing the growth material is performed under a first deposition condition; and
(b) if a first yield of the first plurality of identical semi-

conductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a second deposition condition.

[c2] 2. The method of claim 1, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a third deposition condition.

[c3] 3. The method of claim 2, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein $T1 < T2 < T3$.

[c4] 4. The method of claim 2, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein $P1 > P2 > P3$.

[c5] 5. The method of claim 1, wherein the first and second deposition conditions comprise first and second temperatures, namely, T1 and T2, respectively, and wherein T1 < T2.

[c6] 6. The method of claim 1, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein P1 > P2.

[c7] 7. The method of claim 6, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein F1 > F2.

[c8] 8. The method of claim 1, wherein the first and third regions comprise single-crystal silicon.

[c9] 9. The method of claim 1, wherein the growth material comprises silicon and germanium.

[c10] 10. The method of claim 1, wherein the second region comprises a dielectric material.

[c11] 11. The method of claim 1, wherein the fourth region comprises a polysilicon material.

[c12] 12. The method of claim 1, further comprising the step

of forming a seed layer on top of the second region before the step of depositing the growth material, whereas the seed layer comprises a same material as the fourth region.

[c13] 13. The method of claim 12, wherein the step of forming the seed layer comprises the steps of:
depositing the seed layer on top of both the first and second regions; and
removing a portion of the seed layer on top of the first region.

[c14] 14. A method for forming semiconductor structures, the method comprising the steps of:
(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:
(i) forming a first single-crystal semiconductor region and first and second shallow trench isolation regions on a semiconductor substrate, wherein the first single-crystal semiconductor region is sandwiched between the first and second shallow trench isolation regions, and
(ii) depositing a growth material simultaneously (A) on top of the first single-crystal semiconductor region to grow a second single-crystal semiconductor region from the first single-crystal semiconductor region and (B) on top of the first and second shallow trench isolation re-

gions to grow first and second polysilicon regions from the first and second shallow trench isolation regions, respectively,

wherein the second single-crystal semiconductor region and the first polysilicon region are in direct physical contact with each other,

wherein the second single-crystal semiconductor region and the second polysilicon region are in direct physical contact with each other, and

wherein the step of depositing the growth material is performed under a first deposition condition; and

(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a second deposition condition.

[c15] 15. The method of claim 14, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is

formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a third deposition condition.

[c16] 16. The method of claim 15, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein $T1 < T2 < T3$.

[c17] 17. The method of claim 15, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein $P1 > P2 > P3$.

[c18] 18. The method of claim 14, wherein the first and second deposition conditions comprise first and second temperatures, namely, T1 and T2, respectively, and wherein $T1 < T2$.

[c19] 19. The method of claim 14, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein $P1 > P2$.

[c20] 20. The method of claim 19, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein $F1 > F2$.

[c21] 21. A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) providing a silicon substrate,

(ii) forming a single-crystal silicon layer on the substrate,

(iii) forming first and second shallow trench isolation regions in the single-crystal silicon region, the first and second shallow trench isolation regions defining a first single-crystal silicon region sandwiched between the first and second shallow trench isolation regions,

(iv) growing a seed layer of polysilicon on top of the first and second shallow trench isolation regions, and

(v) depositing silicon and germanium simultaneously (A) on top of the first single-crystal silicon region so as to grow a second single-crystal silicon region and (B) on top of the first and second shallow trench isolation regions so as to grow first and second polysilicon regions, respectively,

wherein the second single-crystal silicon region and the first polysilicon region are in direct physical contact with each other,

wherein the second single-crystal silicon region and the second ploy-silicon region are in direct physical contact

with each other, and

wherein the step of depositing silicon and germanium is performed under a first deposition condition; and

(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a second deposition condition.

[c22] 22. The method of claim 21, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a third deposition condition.

[c23] 23. The method of claim 22, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein $T1 < T2 < T3$.

[c24] 24. The method of claim 22, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein P1 > P2 > P3.

[c25] 25. The method of claim 21, wherein the first and second deposition conditions comprise first and second temperatures, namely, T1 and T2, respectively, and wherein T1 < T2.

[c26] 26. The method of claim 21, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein P1 > P2.

[c27] 27. The method of claim 26, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein F1 > F2.

[c28] 28. A method for determining a fabrication condition for a semiconductor structure design, the method comprising the steps of:
(a) providing a relationship between a yield of the semiconductor structure design, a deposition temperature, and a precursor flow rate, wherein the semiconductor structure design comprises:

(i) a first region and a second region, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface, and

(ii) a third region and a fourth region being on top of the first and second regions, respectively, wherein the third and fourth regions are grown by a step of depositing a growth material simultaneously on top of the first and second regions such that a second common interface surface between the third and fourth region grows from the first common interface surface,

wherein the first and third regions comprise a same material and have single-crystal atoms arrangement,

wherein the first region has a different atoms arrangement than the fourth region, and

wherein the step of depositing the growth material is performed under the deposition temperature and the precursor flow rate;

(b) selecting a target yield for the semiconductor structure design; and

(c) determining a desired deposition temperature and a desired precursor flow rate under which the step of depositing the growth material would form a plurality of identical semiconductor structures according to the semiconductor structure design having the target yield, wherein the desired deposition temperature and the de-

sired precursor flow rate are determined based on the relationship.

[c29] 29. The method of claim 28, wherein the target yield is a maximum yield.

[c30] 30. The method of claim 28, wherein the step of providing the relationship between the yield of the semiconductor structure design, the deposition temperature, and the precursor flow rate comprises the steps of:
forming N sets of multiple identical semiconductor structures according to the semiconductor structure design, wherein for each set of the N sets of multiple identical semiconductor structures, the step of depositing the growth material is performed under a deposition temperature and a precursor flow rate such that there are N deposition temperatures and N precursor flow rates associated with the N sets of multiple identical semiconductor structures, and wherein N is a positive integer;
determining N yields of the N sets of multiple identical semiconductor structures; and
providing the relationship between the yield of the semiconductor structure design, the deposition temperature, and the precursor flow rate based on the N yields, the N deposition temperatures, and N precursor flow rates.

[c31] 31. The method of claim 28, wherein the step of determining the desired deposition temperature and the desired precursor flow rate comprises the steps of:
selecting a target deposition temperature as the desired deposition temperature; and
determining the desired precursor flow rate based on the target yield, the target deposition temperature, and the relationship.

[c32] 32. The method of claim 28, wherein the step of determining the desired deposition temperature and the desired precursor flow rate comprises the steps of:
selecting a target precursor flow rate as the desired precursor flow rate; and
determining the desired deposition temperature based on the target yield, the target precursor flow rate, and the relationship.